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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,097	11/26/2003	Masanori Matsuura	60188-720	6177

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EXAMINER	
KIM, DANIEL Y	
ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 01/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,097	MATSUURA, MASANORI	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Toda (US PGPub No. 20030041224).

For claim 1, Toda discloses a storage device, comprising:

a memory (a memory board system including one controller and a plurality of memory modules, par. 0071);

a microcomputer for taking in data read from the memory according to a externally-supplied clock signal or a clock signal generated based on the externally-supplied clock signal (each memory module generates internal clock signals synchronizing with external clock signals, par. 0071);

a timing signal output circuit for outputting a timing signal indicative of a timing that is shifted by a predetermined time period from a predetermined edge in a read control signal which is used for controlling reading of data from the memory (a predetermined delay time is added to or subtracted from each internal clock signal,

thereby adjusting the timing of the internal clock signals. By using the internal clock signals whose timings are adjusted, data read and write timings are adjusted in each memory module, par. 0071); and

a read data control circuit for performing control such that the microcomputer takes in the data read from the memory based on the timing signal only when the clock signal has a predetermined frequency (a clock signal frequency of 500 MHz is the limit by which data transfer can be normally performed, par. 0016).

For claim 2, Toda discloses the read data control circuit controls based on the timing signal at least any one of the followings:

whether or not the data read from the memory is output to the microcomputer;

the timing for outputting the data read from the memory to the microcomputer (if the memory module is to output data, the data must be output by further advancing the phase from the clock signal. If this is the case, the control signal is set by a command from the controller such that the data output timing is earlier than an internal clock signal synchronizing with the clock signal, thereby allowing the memory controller to correctly load the data, par. 0145);

the timing for taking the data read from the memory into the microcomputer.

For claim 3, Toda discloses the read data control circuit controls whether or not the data read from the memory is output to the microcomputer based on the relationship between the timing which is indicated by the timing signal and the timing at which an edge subsequent to the predetermined edges occurs in the read control signal (par. 0145).

For claim 4, Toda discloses when the read data control circuit does not output the data read from the memory to the microcomputer, the read data control circuit outputs data different from the data read from the memory (instead, a memory module can previously have a data pattern as fixed data. The data pattern is read out from the memory module by a command from the controller in synchronism with a clock signal having a normal frequency. Consequently, the data pattern is output as burst data from the memory module to the data bus line, par. 0151-0152, fig. 18).

For claim 5, Toda discloses the read data control circuit outputs the data read from the memory to the microcomputer for a predetermined time period that is determined according to the timing signal (the controller gives a command to this memory module to shift the position of the control signal to the right or left, thereby adjusting the timing of the internal clock signal, par. 0152; the timing of the internal clock signal, which is output from the internal clock signal generating circuit and used to output data to a data bus line, is adjusted by a procedure, par. 0150).

For claim 6, Toda discloses the read data control circuit outputs data different from the data read from the memory during a time period other than the predetermined time period (the controller gives a command to this memory module to shift the position of the control signal to the right or left, thereby adjusting the timing of the internal clock signal, the flow then returns and the data pattern is read out from the memory module, par. 0152).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7-8 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toda (US PGPub No. 20030041224) and Chheda (US PGPub No. 20030233562).

For claim 7, Toda discloses the invention as per the rejection of claim 2 above. Toda does not, however, expressly disclose a mask circuit for the outputting of the data read from the memory to the microcomputer for a predetermined time period, wherein the read data control circuit performs control such that the microcomputer takes in data output from the mask circuit at a predetermined timing that is determined according to the timing signal.

Chheda, however, discloses a mask circuit for masking the read/write signal to the memory, where there is a single read/write line, then the circuit can disable a read or a write to the memory (par. 0017).

Chheda and Toda are analogous art in that they are of the same field of endeavor, that is, a system and method for controlling memory, especially for limited access to different parts of memory for security reasons. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a mask circuit for this function, because this would allow the invention to selectively allow access to data stored in a memory location, and further aid in preventing an unauthorized agent from reading or altering data (par. 0003-0004), as taught by Chheda.

Claim 8 is rejected using the same rationale as for the rejection of claims 6 and 7 above.

Claim 11 is rejected using the same rationales as for the rejections of claims 1 and 7 above.

For claim 12, the combined teachings of Today and Chheda disclose the invention as per the rejection of claim 11 above. Toda further discloses the timing control circuit sets the predetermined time period during which the mask circuit outputs the data read from the memory and the timing for taking the data output from the mask circuit into the microcomputer, based on a predetermined signal output from the microcomputer (a variable delay circuit for receiving an output signal and outputting the output signal from a delay circuit after delaying the signal by a time corresponding to a control signal, par. 0020).

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Toda (US PGPub No. 20030041224) and Chevallier (US Patent No. 6,002,627).

For claim 9, Toda discloses the invention as per the rejection of claim 1 above. Toda does not, however, expressly disclose a temperature detection circuit that detects a predetermined temperature.

Chevallier, however, discloses an integrated memory device comprising a temperature detection circuit for tracking a temperature of the integrated memory device and producing an output signal on an output node... and a control circuit coupled to the temperature detection circuit for receiving the output signal and adjusting an operation

parameter of the integrated circuit memory device in response to the output signal (col. 1, lines 42-49).

Chevallier and Toda are analogous art in that they are of the same field of endeavor, that is, a system and method for performing a memory control operation, especially based on a trigger event or criterion. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a temperature detection circuit to determine a predetermined temperature because the output of the detection circuit my be used to adjust a memory operation, such as operating frequency (col. 6, lines 41-49), as taught by Chevallier.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Toda (US PGPub No. 20030041224) and Koh (US Patent No. 6,437,308).

For claim 10, Toda discloses the invention as per the rejection of claim 1 above. Toda does not, however, expressly disclose a light detection circuit that detects light having a predetermined intensity.

Koh, however, discloses a light detection circuit employed in an electronic device, such as a portable transaction card (col. 1, lines 8-10), which includes comparing a sensing circuit output with a reference voltage and generating an output (col. 2, lines 40-42).

Koh and Toda are analogous art in that they are of the same field of endeavor, that is, a system and method for memory control, especially based on a trigger event or criterion. It would have been obvious to a person of ordinary skill in the art at the time of

the invention to include a light detection circuit that detects light having a predetermined intensity in the presently claimed invention because this would allow for securing of information, and for operations for processing and storing information from the card to be inhibited (col. 1, lines 34-39), as taught by Koh.

Citation of Pertinent Prior Art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Akagi (US Patent No. 6,434,096) discloses a temperature sensor detects the current apparatus temperature and triggers an operation after comparison of detected temperature to previous detections.

Matsuda (US PGPub No. 20020060659) discloses a trigger occurs in the reflected light detection circuit when reflected light of a predetermined intensity is detected by an apparatus for detecting light.

Contact Information

8. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 8:30am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, is also reachable at 571-272-4210.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

1-6-05

PIERRE VITAL
PRIMARY EXAMINER